

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
AL-255APPLN. NO.
10/655,853INFORMATION DISCLOSURE
STATEMENT BY APPLICANTAPPLICANT
Gregory StarrCONF. NO.
7257FILING DATE
September 5, 2003GROUP ART UNIT
2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>AN</i>	Re. 35,797	5/1998	Graham et al.	326	40	
	3,473,160	10/1969	Wahlstrom	326	41	
	4,494,021	1/1985	Bell et al.	307	591	
	4,633,488	12/1986	Shaw	375	120	
	4,719,593	1/1988	Threewitt et al.	364	900	
	4,857,866	8/1989	Tateishi	331	1A	
	4,868,522	9/1989	Popat et al.	331	2	
	4,959,646	9/1990	Podkowa et al.	340	825.83	
	5,072,195	12/1991	Graham et al.	331	2	
	5,075,575	12/1991	Shizukuishi et al.	307	465	
<i>AN</i>	5,079,519	1/1992	Ashby et al.	331	1A	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	
<i>AN</i>	0 266 065	5/1988	European Pat. Off.	—	—	✓	
<i>AN</i>	0 416 930	3/1991	European Pat. Off.	—	—	✓	
<i>AN</i>	0 778 517	6/1997	European Pat. Off.	—	—	✓	
<i>AN</i>	0 987 822	3/2000	European Pat. Off.	—	—	✓	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
<i>AN</i>	Advanced Micro Devices, Inc., "Am2971 Programmable Event Generator (PEG)," Publication No. 05280, Rev. C, Amendment /0, pp. 4-286 - 4-303 (July 1986)
	Advanced Micro Devices, Inc., "AmPAL*22S8 20-Pin IMOX PAL-Based Sequencer," Publication No. 06207, Rev. B, Amendment /0, pp. 4-102 - 4-121 (October 1986)
	Agere Systems, Inc., "ORCA ORT82G5 0.622/1.0-1.25/2.0-2.5/3.125 Gbits/s Backplane Interface FPSC," Preliminary Data Sheet, pp. 1-35 (July 2001)
	Agere Systems, Inc., "ORCA 8850 Field-Programmable System Chip (FPSC) Eight Channel x 850 Mbits/s Backplane Transceiver," Product Brief, pp. 1-6 (July 2001)
<i>AN</i>	Agere Systems, Inc., "ORCA 8850 Field-Programmable System Chip (FPSC) Eight Channel x 850 Mbits/s Backplane Transceiver," Product Brief, pp. 1-36 (August 2001)

EXAMINER

LLM

DATE CONSIDERED

9/21/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO-9149

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
RL	5,121,014	6/1992	Huang	327	276	
	5,133,064	7/1992	Hotta et al.	395	550	
	5,204,555	4/1993	Graham et al.	307	465	
	5,208,557	5/1993	Kersh	331	57	
	5,239,213	8/1993	Norman et al.	326	38	
	5,349,544	9/1994	Wright et al.	364	600	
	5,394,116	2/1995	Kasturia	331	34	
	5,397,943	3/1995	West et al.	326	39	
	5,418,499	5/1995	Nakao	331	57	
	5,420,544	5/1995	Ishibashi	331	11	
RL	5,424,687	6/1995	Fukuda	331	11	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
RL	1 056 207	11/2000	European Pat. Off.	—	—		
RL	1-137646	5/1989	Japan	—	—	✓	
RL	10,215,156	8/1998	Japan Pat. Abstract	—	—	✓	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
RL	DynaChip Corp., "Application Note: Using Phase Locked Loops in DL6035 Devices" (1998)
RL	DynaChip Corp., DY6000 Family Datasheet (December 1998)
RL	Ko, U., et al., "A 30-ps Jitter, 3.6 µs Locking, 3.3-Volt Digital PLL for CMOS Gate Arrays," <u>Proceedings of the IEEE 1993 Custom Integrated Circuits Conference</u> , Publication No. 0-7803-0826-3/93, pp. 23.3.1-23.3.4 (May 9-12, 1993)
RL	LSI Logic Corp., 500K Technology Design Manual (Document DB04-000062-00, First Edition), pp. 8-1 - 8-33 (December 1996)
RL	Lucent Technologies, Inc., "Optimized Reconfigurable Cell Array (ORCA®) OR3Cxxx/OR3Txxx Series Field-Programmable Gate Arrays, Preliminary Product Brief, (November 1997)

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FORM PTO-6449

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U.S. PATENT DOCUMENTS

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<i>Au</i>	5,448,191	9/1995	Meyer	327	105	
	5,477,182	12/1995	Huizer	327	261	
	5,506,878	4/1996	Chiang	377	39	
	5,542,083	7/1996	Hotta	709	400	
	5,581,214	12/1996	Iga	331	16	
	5,629,651	5/1997	Mizuno	331	34	
	5,642,082	6/1997	Jefferson	331	25	
	5,646,564	7/1997	Erickson et al.	327	158	
	5,656,959	8/1997	Chang et al.	327	105	
	5,691,669	11/1997	Tsai et al.	331	17	
<i>Au</i>	5,699,020	12/1997	Jefferson	331	17	

FOREIGN PATENT DOCUMENTS

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						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	DOCUMENT
<i>Au</i>	Lucent Technologies, Inc., "ORCA® Series 3 Field-Programmable Gate Arrays, Preliminary Data Sheet, Rev. 01 (August 1998)
	Monolithic Memories, Inc., "Programmable Array Logic PAL20RA10-20 Advance Information," pp. 5-95 - 5-102 (January 1988)
	National Semiconductor Corp., LVDS Owner's Manual & Design Guide (April 25, 1997)
	National Semiconductor Corp., "DS90CR285/DS90CR286 +3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-66 MHZ," (March 1998)
<i>Au</i>	Xilinx, Inc., "Virtex 2.5V Field Programmable Gate Arrays Advance Product Specification (Version 1.0) (October 20, 1998)

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9/21/04

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. AL-255	APPLN. NO. 10/655,853
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Gregory Starr	CONF. NO. 7257
		FILING DATE September 5, 2003	GROUP ART UNIT 2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
KY	5,742,180	4/1998	DeHon et al.	326	40	
	5,744,991	4/1998	Jefferson et al.	327	158	
	5,777,360	7/1998	Rostoker et al.	257	315	
	5,815,016	9/1998	Erickson	327	158	
	5,847,617	12/1998	Reddy et al.	331	57	
	5,889,436	3/1999	Yeung et al.	331	2	
	5,900,757	5/1999	Aggarwal et al.	327	198	
	5,952,891	9/1999	Boudry	331	57	
	5,963,069	10/1999	Jefferson et al.	327	158	
	5,970,110	10/1999	Li	377	48	
tu	5,974,105	10/1999	Wang et al.	375	376	

FOREIGN PATENT DOCUMENTS

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						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
ta	Xilinx, Inc., "Application Note: Using the Virtex Delay-Locked Loop (Version 1.31) (October 21, 1998)
ta	Zaks, R., et al., <u>From Chips to Systems: An Introduction to Microcomputers</u> , pp. 54-61 (Prentice-Hall, Inc., Englewood Cliffs, N.J., 1987)

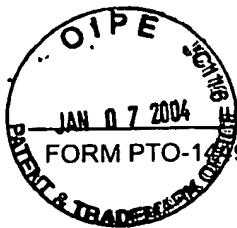
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7/21/04

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FORM PTO-169

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U.S. PATENT DOCUMENTS

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AG	5,987,543	11/1999	Smith	710	70	
/	5,999,025	12/1999	New	327	156	
/	6,014,048	1/2000	Talaga, Jr., et al.	327	156	
/	6,043,677	3/2000	Albu et al.	326	39	
/	6,069,506	5/2000	Miller, Jr., et al.	327	156	
/	6,069,507	5/2000	Shen et al.	327	156	
/	6,104,222	8/2000	Embree	327	156	
/	6,114,915	9/2000	Huang et al.	331	25	
/	6,141,394	10/2000	Linebarger et al.	375	376	
/	6,144,242	11/2000	Jeong et al.	327	269	
AG	6,157,266	12/2000	Tsai et al.	331	57	

FOREIGN PATENT DOCUMENTS

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						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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Sheet 6 of 6

FORM PTO-1649

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U.S. PATENT DOCUMENTS

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XW	6,249,189	6/2001	Wu et al.	331	18	
	6,252,419	6/2001	Sung et al.	326	38	
	6,278,332	8/2001	Nelson et al.	331	17	
	6,320,469	11/2001	Friedberg et al.	331	1A	
	6,373,278	4/2002	Sung et al.	326	38	
	6,411,150	6/2002	Williams	327	281	
	6,462,623	10/2002	Horan et al.	331	17	
	6,483,886	11/2002	Sung et al.	375	376	
AC	2001/0033188 A1	10/2001	Aung et al.	327	141	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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